REMARKS

Upon entry of this Amendment, claims 1-10 and 15-27 will be pending in the present application. Claims 11-14 are canceled. Claims 1, 6, 15, 21 and 22 are independent claims. Claims 4-7, 10, 16, 18 and 19 are amended by this reply.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-3, 6-8, 11, 12, 13, 14, 15, 16, 21, 22 and 26 stand rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,994,721 to Zhong et al. (Zhong) for the reasons set forth in paragraph 1 of the Office Action. The rejection is respectfully traversed.

Claims 1-3, 6-8, 15, 16, 21, 22 and 26

Zhong teaches in Figure 4, a drain electrode 13 made up of drain metal layer 29, source metal layer 31 and insulating color filters 101, 102, 103 or 104. An opening 35 is formed in the color filter, and pixel electrode 3 is formed in the opening. Zhong, however, does not disclose a planarization layer formed on the TFT or the color filter. In Zhong, the color filter is distinct from the planarization layer. Reference numeral 101 noted by the Examiner as designating a planarization layer, instead properly designates a color filter.

Therefore, Zhong does not teach a planarization layer over the color filter layer and the source and the drain electrodes, the planarization layer having an opening exposing the drain electrode thereunder; and a pixel electrode on the planarization layer and electrically connected with the drain electrode via the opening in the planarization layer as recited in independent claim 1 and similarly stated in independent claims 6, 15, 21 and 22.

Claims 2, 3, 7, 8, 16 and 26 dependent on claims 6, 15, 21 and 22 are patentable at least for the reasons stated with respect to claims 1, 6, 15, 21 and 22. Accordingly, withdrawal of this art grounds of rejection is respectfully requested.

Claim Rejections Under 35 U.S.C. § 103

Zhong in View of Kashiwazaki

Claims 4, 5, 9, 10, 17, 23 and 25 stand rejected under 35 U.S.C. § 103(a) over Zhong in view of U.S. Patent No. 6,162,510 to Kashiwazaki et al. (Kashiwazaki), for the reasons set forth in paragraph 2 of the Office Action. The rejection is respectfully traversed.

Kashiwazaki discloses a gate electrode 102, a gate insulating film 103, a silicon film 104, and an etching stop layer 105. Kashiwazaki does not disclose (in Figure 2) a light shield 11 below the gate electrode. Even if Kashiwazaki disclosed

or suggested the light shield 11 in Figure 2, Kashiwazaki like Zhong (argued above) does not disclose a planarization over the color filter and the source and the drain electrodes, the planarization layer having an opening exposing the drain electrode thereunder; and a pixel electrode on the planarization layer and electrically connected with the drain electrode via the opening in the planarization layer as recited in independent claim 1, and similarly stated in independent claims 6, 15, 21 and 22.

Claims 4, 5, 9, 10, 17, 23 and 25 are dependent on claims 1, 6, 15, 21 and 22. Therefore, Zhong in view of Kashiwazaki cannot render claims 4, 5, 9, 10, 17, 23 and 25 obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection is respectfully requested.

Zhong in View of Oike

Claims 19, 20 and 27 stand rejected by the Examiner under 35 U.S.C. § 103(a) over Zhong in view of U.S. Patent No. 6,104,459 to Oike, for the reasons set forth in paragraph 3 of the Office Action. The rejection is respectfully traversed.

Oike discloses (in Figure 7) an active layer 51a. The source and drain regions, however, are not shown to be formed at the end portions of the active layer, and any separation therebetween is indiscernible. Even so, Oike like Zhong (argued above) does not disclose or suggest a planarization layer over the color

filter layer and the source and the drain electrodes, the planarization layer having an opening exposing the drain electrode thereunder; and a pixel electrode on the planarization layer and electrically connected with the drain electrode via the opening in the planarization layer, as recited in independent claim 1 and similarly stated in independent claims 15 and 22.

Claims 19, 20 and 27 depend on claims 15 and 22. Therefore Zhong in view of Oike cannot render claims 19, 20 and 27 obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection is respectfully requested.

Zhong in view of Nishikawa

Claims 18 and 24 stand rejected by the Examiner under 35 U.S.C. §103(a) over Zhong in view of U.S. Patent No. 5,724,107 to Nishikawa et al. (Nishikawa) for the reasons set forth in paragraph 4 of the Office Action. The rejection is respectfully traversed.

Nishikawa is directed to providing a liquid crystal display which improves aperture ratio and increases storage capacitance. Assuming for the sake of argument, that Nishikawa discloses or suggests the light shielding layer of claims 18 and 24, it remains that Nishikawa, like Zhong, (argued above) does not disclose or suggest a planarization layer over the color filter layer and the source and the

drain electrodes, the planarization layer having an opening exposing the drain electrode thereunder; and a pixel electrode on the planarization layer and electrically connected with the drain electrode via the opening in the planarization layer as recited in independent claim 1 and similarly stated in independent claims 15 and 22.

Claims 18 and 24 are dependent claims 15 and 22. Therefore Zhong in view of Nishikawa cannot render claims 18 and 24 obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

CONCLUSION

Applicant points out that all of the Examiner's comments have been addressed and that all of the Examiner's objections and rejections have been overcome, thereby placing all claims pending in the present Application in condition for allowance. Allowance of the claims is respectfully solicited.

In the event that any outstanding matters remain in this application, Applicant requests that the Examiner contact the undersigned at (703) 205-8000 to discuss such matters.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By [signature] Reg No 32,334
for Joseph A. Kolasch
Reg. No. 22,463

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

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Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning on page 2, line 5, has been amended as follows:

--Figs. 2A to 2D are cross sectional views illustrating a process of manufacturing a conventional LCD device having the COT structure. First, as shown in Fig. 2A, a gate electrode 50 is formed on the substrate 1. A gate insulating layer 52 is formed over the whole substrate 1 while covering the gate electrode 50. A semiconductor layer 54 is formed on the gate insulating layer 52. The source and drain electrodes 56 and 58 are spaced apart from each other and overlap both end portions of the semiconductor layer 54, respectively. A passivation film 60 is formed over the whole substrate 1 while covering the source and drain electrodes 56 and 58 and the semiconductor layer 54. The semiconductor layer 54 includes an amorphous silicon layer and a doped semiconductor layer. A portion of the doped semiconductor layer between the source [an] and drain electrodes is etched to form a channel region.--

The paragraph beginning on page 4, line 20, has been amended as follows:

--In a third preferred embodiment, the thin film transistor further includes: an active layer having source and drain regions at both end portions thereof; a

gate insulating layer on a central portion of the active layer other than the source and drain regions; a gate electrode formed on the gate insulating layer; and an inter layer insulator formed over the substrate, having first and second contact holes for respectively exposing a portion of the source and drain regions, wherein the source and drain electrodes are formed on the inter layer insulator to respectively contact with the source and drain regions. The active layer can be made of polysilicon. The liquid crystal display device may include a light shielding layer formed between the substrate and the thin film transistor and an insulating layer covering the light [shileding] shielding layer.--

The paragraph beginning on page 6, line 9, has been amended as follows:

--In a third preferred embodiment, the method further includes forming a light shielding layer before forming the thin film transistor; and forming an insulating layer for covering the light shielding layer. The active layer can be made of amorphous silicon. Forming the thin film transistor includes: forming a pure semiconductor layer; forming a gate insulating layer, a width of the gate insulating layer being smaller than the pure semiconductor layer; forming a gate electrode on the gate insulating layer; ion-doping an exposed portion of the pure semiconductor layer to define source and drain regions; forming an [inter layer] interlayer insulator over the substrate, the [inter layer] interlayer including a

source region contact hole on a portion of the source electrode and a drain region contact hole on a portion of the drain electrode; and forming source and drain [electrodes] electrodes, the source and drain [electrdoes] electrodes electrically contacting with the source and [drian] drain regions, respectively. The pure semiconductor layer can be made of polysilicon.--

The paragraph beginning on page 8, line 10, has been amended as follows:

--Fig. 6 is a plan view illustrating an array substrate for use in a liquid crystal display according to the present invention. The array substrate has gate lines 101a in a transverse direction, data lines 101b arranged in a longitudinal direction perpendicular to the gate lines 101a. Patterns of the semiconductor layer and pixel electrode are not shown for simplicity. Figs. 3A to 5E are cross sectional views taken along line I-II of Fig. 6, illustrating fabrication process steps of an array substrate having color filters according to the present invention.--

The paragraph beginning on page 9, line 9, has been amended as follows:

--Then, as shown in Fig. 3C and Fig. 6, a color filter 112 including color filter layers R(red), G(green) and B(blue) is formed in a stripe shape. In order to form the color filter 112 including the color filter layers of R, G and B, a process of depositing a color resin and pattering it is repeated three times. At this point, the

color filter 112 for each TFT overlaps an side portion of the data line 101b and an end portion of the drain electrode 108, denoted as the regions "T" in Fig. 3C, so as to prevent light leakage and to improve an aperture ratio. Because boundary of adjacent color filter stripes is located on the center portion of the data line, it can provide a sharp, immutable boundary between color filter stripe. Bleeding of adjoining color filters to each other and blurring of boundaries can be also avoided. The color filter can [be] overlap a portion of source electrode 106. Thereafter, using the source and drain electrodes 106 and 108 as a mask, a portion of the doped amorphous silicon layer 104b between the source and drain electrodes 106 and 108 is etched by a dry[-] or a wet-etching technique to form a channel region.--

The paragraph beginning on page 11, line 6, has been amended as follows:

--A third preferred embodiment of the present invention relates to an LCD device having the COT structure and using a coplanar type TFT as a switching element. Figs. 5A to 5E are cross sectional views illustrating a process of manufacturing the LCD device according to the third preferred embodiment of the present invention. First, as shown in Fig. 5A, a light shielding layer 200 is formed on a substrate 1. The light shielding layer 200 serves to protect an active layer

204[, which will be formed in later step,] from light. A first insulating layer 202 is formed on the substrate 1 while covering the light shielding layer 200.--

The paragraph beginning on page 12, line 1, has been amended as follows:

--Subsequently, as shown in Fig. 5C, a third insulating layer 210 is formed over the whole substrate 1. The third insulating layer 210 serves as an [inter layer] interlayer insulator. The third insulating layer 210 includes source and drain contact holes 212 and 214 to respectively expose the source and drain regions 204c and 204d.--

The paragraph beginning on page 12, line 5, has been amended as follows:

--Next, as shown in Fig. 5D, source and drain electrodes 216 and 218 are formed on the third insulating layer 210 and are electrically connected with the source and drain regions 204c and 204d through the source and drain contact holes 212 and 214, respectively. Thereafter, a color filter 220 (including the color filter layers R, G and B) is formed to respectively overlap side portions of the data line 101b and drain electrode 218. In other words, the color filter layers R overlap side portions of the data line 101b, and the color filter layers G overlap end portions of the drain electrode 218 as shown in Fig. 6. The color filter can be overlap a portion of source electrode 216. The reason for this overlap is to prevent

[a] light leakage, to improve an aperture ratio and to have sharp a boundary between adjoining two color filter stripes.--

In the Claims:

The claims have been amended as follows:

4.(Amended) The device of claim 1, [wherin] wherein the semiconductor layer comprises:

a first layer on the insulation layer;

an etch stop layer on the first layer; and

a second layer over the first layer and the etch stop layer.

5. (Amended) The device of claim 1, further comprising a light [sheilding] shielding layer below the gate electrode.

6. (Amended) A method of forming liquid crystal display (LCD) device, the method comprising:

[foming] forming a substrate;

forming a gate electrode over the substrate;

forming an insulation layer on the gate electrode and the substrate;

forming a semiconductor layer, aligned relative to the gate electrode, on the insulating layer;

forming a source electrode and a drain electrode electrically connected with the semiconductor layer;

forming a color filter layer on and in direct contact with the source and the drain electrodes;

forming a planarization layer over the color filter layer and the source and [the] drain electrodes, the planarization layer having an opening exposing the drain electrode thereunder; and

forming a pixel electrode on the planarization layer and electrically connected with the drain electrode via the opening in the planarization layer.

7. (Amended) The method of claim 6, wherein the color filter layer is formed to substantially [covers] cover the source and drain electrodes to prevent light leakage.

10. (Amended) The method of claim 6, further comprising a step of forming a light [sheilding] shielding layer below the gate electrode.

16. (Amended) The liquid crystal display device of claim 15, wherein the TFT further includes:

a gate insulating layer on the substrate and covering the gate electrode; and

a semiconductor layer formed on the gate insulating layer, having an amorphous silicon layer and a doped amorphous silicon layer,

wherein the gate electrode is formed on the substrate, while the source and [drian] drain electrodes are spaced apart from one another and overlap end portions of the [doepd] doped amorphous silicon layer, respectively.

18. (Amended) The liquid crystal display device of claim 15, further comprising:

a light shielding layer formed between the substrate and the TFT; and

an insulating layer covering the light [shileding] shielding layer.

19. (Amended) The liquid crystal display device of claim 15, wherein the TFT further includes:

an active layer having source and drain regions at end portions;

a gate insulating layer on a central portion of the active layer, the gate electrode being formed on the gate insulating layer; and

an [inter layer] interlayer insulator formed entirely over the substrate, having a first and a second contact hole which respectively expose a portion of the source and drain regions therebelow,

wherein the source and drain electrodes are formed on the [inter layer] interlayer insulator to respectively contact the source and drain regions.